Amendments To The Claims

The following list of the claims replaces all prior versions and lists of the claims in this application.

1. (Currently amended) A structure for corners of metallic features of semiconductor ~~integrating~~ integrated circuits, comprising:

~~corner angles of all corners of~~ metallic features[[,]] imbedded in dielectric layers, ~~which~~ wherein corner angles of all corners of the metallic features are greater than 90 degrees.

2. (Previously presented) The structure of claim 1 wherein one of said dielectric layers includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, PSG, and BPSG.

3. (Previously presented) The structure of claim 1 wherein one of said dielectric layers is a composite of dielectric layers.

4. (Previously presented) The structure of claim 1 wherein one of said dielectric layers is a low-K dielectric material.

5. (Previously presented) The structure of claim 1 wherein one of said metallic features includes a material selected from the group consisting of doped polysilicon, metal silicides, Al, Cu, and W.

6. (Previously presented) The structure of claim 1 wherein one of said metallic features is a feature selected from the group consisting of via, trench, pad, and line.

7. (Currently amended) A structure for corners of metallic features of semiconductor ~~integrating~~ integrated circuits, comprising:

~~Corners of all~~ metallic features[[,]] imbedded in dielectric layers, ~~which~~ wherein corners of all metallic features are formed in n-fold clipped corner configurations, with n being greater than 0.

8. (Previously presented) The structure of claim 7 wherein one of said dielectric layers includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, PSG, and BPSG.

9. (Previously presented) The structure of claim 7 wherein one of said dielectric layers is a composite of dielectric layers.

10. (Previously presented) The structure of claim 7 wherein one of said dielectric layers is a low-K dielectric material.

11. (Previously presented) The structure of claim 7 wherein one of said metallic features includes a material selected from the group consisting of doped polysilicon, metal silicides, Al, Cu, and W.

12. (Previously presented) The structure of claim 7 wherein one of said metallic features is a feature selected from the group consisting of via, trench, pad, and line.

13. (Previously presented) The structure of claim 7 wherein said n-fold clipped corner configurations of corners of metallic features of a level are n-fold equal angle clipped corner configurations, with n equal or greater than one, when said dielectric layer of said level includes a low-K dielectric material and no CMP step is done on said level.

14. (Previously presented) The structure of claim 7 wherein said n-fold clipped corner configurations of corners of metallic features of a level are n-fold equal angle clipped corner configurations, with n equal or greater than 2, when said dielectric layer of said level includes a low-K dielectric material and said level has a structural characteristic resulting from a CMP step.

15. (Previously presented) The structure of claim 7 wherein said n-fold clipped corner configurations of corners of metallic features of a level are n-fold equal angle clipped corner configurations, with n equal or greater than one, when said dielectric layer of said level includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, PSG, and BPSG, and said level has a structural characteristic resulting from a CMP step.

16. (Currently amended) A structure for metallic features of semiconductor ~~integrating~~ integrated circuits, comprising:

shapes of all metallic features imbedded in dielectric layers, that could be formed as squares, are instead configured as m-sided regular polygons, where m is greater than 4.

17. (Previously presented) The structure of claim 16 wherein one of said dielectric layers includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, PSG, and BPSG.

18. (Previously presented) The structure of claim 16 wherein one of said dielectric layers is a composite of dielectric layers.

19. (Previously presented) The structure of claim 16 wherein one of said dielectric layers is a low-K dielectric material.

20. (Previously presented) The structure of claim 16 wherein one of said metallic features includes a material selected from the group consisting of doped polysilicon, metal silicides, Al, Cu, and W.

21. (Previously presented) The structure of claim 16 wherein one of said metallic features is a pad.

22. (Previously presented) The structure of claim 16 wherein m of each said m-sided regular polygon is at least equal to 8 when said metallic features are on a level where said dielectric layer includes a low-K dielectric material and no CMP step is done on said level.

23. (Previously presented) The structure of claim 16 wherein m of each said m-sided regular polygon is at least equal to 16 when said metallic features are on a level where said dielectric layer includes a low-K dielectric material and said level has a structural characteristic resulting from a CMP step.

24. (Previously presented) The structure of claim 16 wherein m of each said m-sided regular polygon is at least equal to 8 when said metallic features are on a level where said dielectric layer includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, PSG, and BPSG, and said level has a structural characteristic resulting from a CMP step.

Claims 25-48 (Canceled).

49. (Previously presented) The structure of claim 4, wherein said dielectric layer has a dielectric constant less than about 3.0.